AMENDMENTS TO THE CLAIMS

Please amend the claims and add new claims as follows:

1-32. (Canceled)

33. (New) A content addressable memory (CAM) device comprising:

a plurality of CAM cells;

a first set of compare lines coupled to the plurality of CAM cells to provide a first compare value thereto;

a priority encoder to generate a match address; and

a second set of compare lines coupled to the plurality of CAM cells and coupled to receive the match address from the priority encoder.

34. (New) The CAM device of claim 33 wherein each of the CAM cells includes a first compare circuit coupled to at least one compare line of the first set of compare lines, and a second compare circuit coupled to at least one compare line of the second set of compare lines.

35. (New) The CAM device of claim 34 further comprising a first set of match lines coupled to the CAM cells, and a second set of match lines coupled to the CAM cells, and wherein the first compare circuit within each of the CAM cells is coupled to a match line of the first set and the second compare circuit within each of the CAM cells is coupled to a match line of the second set.

36. (New) The CAM device of claim 33 wherein the CAM cells are configured to compare data values stored therein simultaneously with the first compare value and with the match

address.

37. (New) The CAM device of claim 36 further comprising:

a first set of match lines coupled to respective rows of the CAM cells to indicate whether the first compare value matches data stored within any of the rows of the CAM cells; and

a second set of match lines coupled to the respective rows of the CAM cells to indicate whether the match address matches data stored within any of the rows of the CAM cells.

38. (New) The CAM device of claim 33 wherein each of the CAM cells comprises an edge-triggered storage element.

39. (New) The CAM device of claim 33 further comprising a plurality of write bit lines coupled to the CAM cells to enable a write data value to be stored within a selected row of the CAM cells.

40. (New) The CAM device of claim 39 further comprising a plurality of read bit lines coupled to the CAM cells to enable a read data value to be read from a selected row of the CAM cells.

41. (New) The CAM device of claim 33 further comprising a plurality of read word lines coupled to respective rows of the CAM cells to enable a data value to be read from a first selected one of the rows of CAM cells.

42. (New) The CAM device of claim 41 further comprising an address circuit to assert at least

one of the plurality of read word lines during a sequence of two or more compare operations within the CAM cells.

43. (New) The CAM device of claim 41 further comprising a plurality of write word lines coupled to the respective rows of the CAM cells to enable a write data value to be written into a second selected one of the rows of CAM cells concurrently with the read data value being read from the first selected one of the rows of CAM cells.

44. (New) The CAM device of claim 43 further comprising an address circuit to concurrently assert one of the plurality of read word lines and one of the plurality of write word lines.

45. (New) A method of operation within a content addressable memory (CAM) device, the method comprising:

generating a first match address within a priority encoder of the CAM device;

outputting the first match address onto a first set of compare lines of a CAM array; and

outputting a first compare value onto a second set of compare lines of the CAM array concurrently with outputting the first match address onto the first set of compare lines.

46. (New) The method of claim 45 further comprising simultaneously comparing the first match address and the first compare value with contents of the CAM array.

47. (New) The method of claim 46 further comprising outputting a data value from the CAM array concurrently with comparing the first match address and the first compare value with contents of the CAM array.

48. (New) The method of claim 47 further comprising generating a second match address within the priority encoder after generating the first match address, and comparing the second match address with contents of the CAM array, and wherein outputting the data value from the CAM array comprises outputting the data value from the CAM array for a duration that spans comparison of the match address with contents of the CAM array and comparison of the second match address with contents of the CAM array.

49. (New) The method of claim 46 further comprising generating match signals on a first set of match lines to indicate results of comparing the first match address with the contents of the CAM array, and generating match signals on a second set of match lines to indicate results of comparing the first compare value with the contents of the CAM array.

50. (New) The method of claim 49 further comprising outputting an error signal if the first match address matches a value stored within the CAM array.

51. (New) The method of claim 45 further comprising generating a sequence of check address values within an address generating circuit, and wherein the first compare value is one of the check address values.

52. (New) A content addressable memory (CAM) device comprising:

a CAM array;

means for generating a first match address;

means for outputting the first match address onto a first set of compare lines of the CAM array; and

means for outputting a first compare value onto a second set of compare lines of the CAM array concurrently with outputting the first match address onto the first set of compare lines.

53. (New) The CAM device of claim 52 further comprising means for simultaneously comparing contents of the CAM array with the first match address and with the first compare value.

54. (New) The CAM device of claim 53 further comprising:

means for generating a first set of match signals to indicate results of comparing the first match address with the contents of the CAM array; and

means for generating a second set match signals to indicate results of comparing the first compare value with the contents of the CAM array.